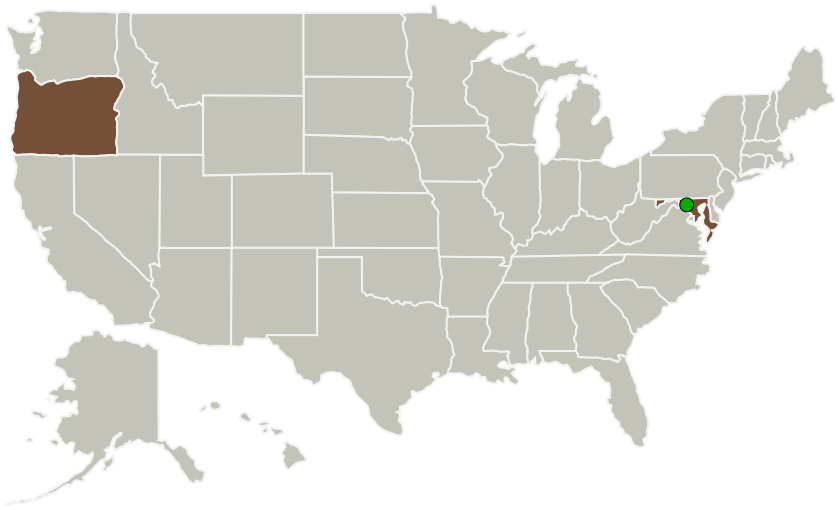
Robust, Wafer-level 3D Electrical Interconnect Technology, Phase I

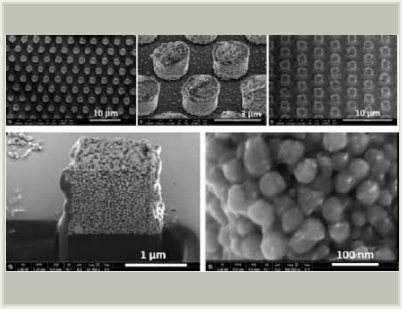
Completed Technology Project (2016 - 2016)

Project Introduction

There is a longstanding need for a reliable, low-cost manufacturing method for high-density three-dimensional (3D) interconnection of integrated circuits (ICs). This includes assembly of 3D stacked electrical interconnection of dissimilar semiconductors, electrical-interconnection of fine-pixel-pitch semiconductor detector arrays with readout ICs (ROICs) at the pixel level, and interconnection of ICs with flexible organic substrates and interposers. Such technology will allow for higher-density circuit integration into small-sized packages and enable high-density focal planes to be developed at lower costs. To address the need for high-density three-dimensional (3D) interconnection of circuits and detectors, including those made of dissimilar materials, inkjet-print additive-manufacturing (AM) materials and deposition technologies will be developed. It will be shown that reliable low-resistance electrical connections can be made- in three dimensions- to vertically stacked integrated circuits and interposers. The process is compatible with wafer-to-wafer, chip-to-wafer, and chip-to-chip processing, requires only modest capital investment, and can be performed with high yields at less cost and finer pitch compared to today's indium-bump hybridization technologies. In Phase I, the ability to produce densely packed conductive sub-1-µm and larger nanometal pillars to form low-resistivity 3D interconnects at a sub-3-µm pitch will be demonstrated. The process technology will be shown capable of forming 2.5D/3D stacked circuits at the chip and wafer levels. Parts will be electrically characterized over a range of frequencies, and samples will be environmentally and mechanically tested.

Primary U.S. Work Locations and Key Partners





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Completed Technology Project (2016 - 2016)

Organizations Performing Work	Role	Type	Location
Voxtel, Inc.	Lead Organization	Industry	Beaverton, Oregon
Goddard Space Flight Center(GSFC)	Supporting Organization	NASA Center	Greenbelt, Maryland

Primary U.S. Work Locations	
Maryland	Oregon

Project Transitions

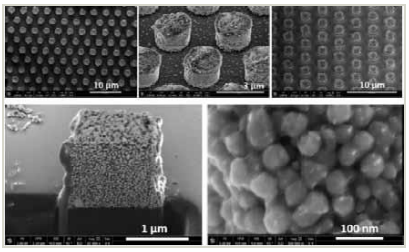
June 2016: Project Start

December 2016: Closed out

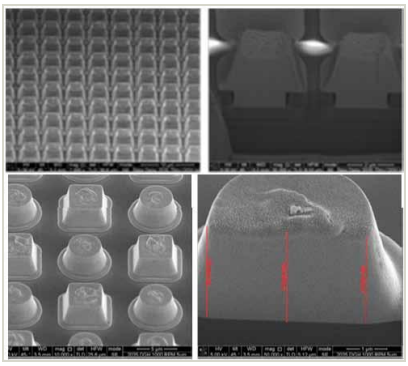
Closeout Documentation:

- Final Summary Chart*(https://techport.nasa.gov/file/139615)*

Images



Briefing Chart Image
Robust, Wafer-level 3D Electrical Interconnect Technology, Phase I
(https://techport.nasa.gov/image/128488)



Final Summary Chart Image
Robust, Wafer-level 3D Electrical Interconnect Technology, Phase I Project Image
(https://techport.nasa.gov/image/127883)

Organizational Responsibility

Responsible Mission Directorate:
Space Technology Mission Directorate (STMD)

Lead Organization:
Voxtel, Inc.

Responsible Program:
Small Business Innovation Research/Small Business Tech Transfer

Project Management

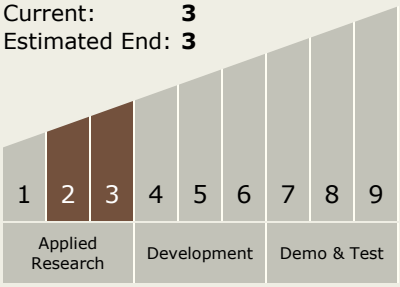
Program Director:
Jason L Kessler

Program Manager:
Carlos Torrez

Principal Investigator:
Ren Earl

Technology Maturity (TRL)

Start: **2**
Current: **3**
Estimated End: **3**



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Completed Technology Project (2016 - 2016)

Technology Areas

Primary:

- TX02 Flight Computing and Avionics
  - TX02.1 Avionics Component Technologies
    - TX02.1.2 Electronic Packaging and Implementations

Target Destinations

The Sun, Earth, The Moon, Mars, Others Inside the Solar System, Outside the Solar System